Amendments to the Claims:

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method comprising maintaining a synchronization state for a local clock generating circuit of a first of a number of components of a distributed system according to a number of local clock cycles recorded between successive occurrences of a global synchronization signal provided to each of the components of the distributed system,

wherein the synchronization state indicates that the local clock generating circuit is synchronized to the global synchronization signal,

wherein the local clock generating circuit can switch between a plurality of states, the plurality of states including the synchronization state, and an alarm state, and

wherein the components comprise line and/or switch cards of a communications switch.

2. (Previously Presented) The method of claim 1 wherein the local clock generating circuit enters the synchronization state only after observing a predetermined number of occurrences of successive local clock cycles between the successive occurrences of the global synchronization signal.

3. (Original) The method of claim 2 wherein the local clock generating circuit provides local control signals for the first of the components at time instants corresponding to the number of local clock cycles.

4. (Original) The method of claim 3 wherein the local clock generating circuit continues to provide local control signals for the first of the components at time instants corresponding to the

number of local clock cycles even after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle more or less than the number of local clock cycles.

5. (Original) The method of claim 3 wherein the local clock generating circuit enters an alarm state when the global synchronization signal is observed at time instants corresponding to more than one local clock cycle more or less than the number of local clock cycles.

6. (Original) The method of claim 3 wherein the local clock generating circuit enters a missing clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle less than the number of local clock cycles.

7. (Original) The method of claim 6 wherein the local clock generating circuit returns to the synchronization state from the missing clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle more than the number of local clock cycles.

8. (Original) The method of claim 6 wherein the local clock generating circuit enters an alarm state from the missing clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one or more local clock cycle less than the number of local clock cycles.

9. (Original) The method of claim 3 wherein the local clock generating circuit enters an extra clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle more than the number of local clock cycles.

10. (Original) The method of claim 9 wherein the local clock generating circuit returns to the synchronization state from the extra clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle less than the number of local clock cycles.

11. (Original) The method of claim 9 wherein the local clock generating circuit enters an alarm state from the extra clock state after an instance of the global synchronization signal is observed at a time instant corresponding to two or more local clock cycles more than the number of local clock cycles.

12. (Currently Amended) A system comprising a number of asynchronous components coupled to one another through one or more communication signal paths, one or more of the components including local clock generating circuits configured to generate local control signals, each of the local clock circuits being synchronized with one another according to a number of local clock cycles recorded between successive occurrences of a global synchronization signal provided to each of the components of the system,

wherein the synchronization state indicates that the local clock generating circuits are synchronized to the global synchronization signal,

wherein the local clock generating circuit can switch between a plurality of states, the plurality of states including the synchronization state, and an alarm state, and

wherein the components comprise line and/or switch cards of a communications switch.

13. (Previously Presented) The system of claim 12 wherein each of the local clock generating circuits is configured to enter the synchronization state only after observing a predetermined

number of occurrences of successive local clock cycles between the successive occurrences of the global synchronization signal.

14. (Original) The system of claim 13 wherein the local clock generating circuits are further configured to continue to provide local control signals for their respective components at time instants corresponding to the number of local clock cycles even after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle more or less than the number of local clock cycles.

15. (Original) The system of claim 13 wherein the local clock generating circuits are configured to enter an alarm state when the global synchronization signal is observed at time instants corresponding to more than one local clock cycle more or less than the number of local clock cycles.

16. (Original) The system of claim 13 wherein the local clock generating circuits are configured to enter a missing clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle less than the number of local clock cycles.

17. (Original) The system of claim 16 wherein the local clock generating circuits are configured to return to the synchronization state from the missing clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle more than the number of local clock cycles.

18. (Original) The system of claim 16 wherein the local clock generating circuits are configured to enter an alarm state from the missing clock state after an instance of the global synchronization

signal is observed at a time instant corresponding to two or more local clock cycles less than the number of local clock cycles.

19. (Original) The system of claim 13 wherein the local clock generating circuits are configured to enter an extra clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle more than the number of local clock cycles.

20. (Original) The system of claim 19 wherein the local clock generating circuits are configured to return to the synchronization state from the extra clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle less than the number of local clock cycles.

21. (Original) The system of claim 19 wherein the local clock generating circuits are configured to enter an alarm state from the extra clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one or more local clock cycle more than the number of local clock cycles.

22. (Cancelled)

23. (Currently Amended) A computer readable medium containing executable instructions which, when executed in a processing system, causes the system to perform a method comprising maintaining a synchronization state for a local clock generating circuit of a first of a number of components of a distributed system according to a number of local clock cycles recorded between successive occurrences of a global synchronization signal provided to each of the components of the distributed system,

wherein the synchronization state indicates that the local clock generating circuit is synchronized to the global synchronization signal,

wherein the local clock generating circuit can switch between a plurality of states, the plurality of states including the synchronization state, and an alarm state, and

wherein the components comprise line and/or switch cards of a communications switch.

24. (Previously Presented) The computer readable medium of claim 23 wherein the local clock generating circuit enters the synchronization state only after observing a predetermined number of occurrences of successive local clock cycles between the successive occurrences of the global synchronization signal.

25. (Previously Presented) The computer readable medium of claim 24 wherein the local clock generating circuit provides local control signals for the first of the components at time instants corresponding to the number of local clock cycles.

26. (Previously Presented) The computer readable medium of claim 25 wherein the local clock generating circuit continues to provide local control signals for the first of the components at time instants corresponding to the number of local clock cycles even after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle more or less than the number of local clock cycles.

27. (Previously Presented) The computer readable medium of claim 25 wherein the local clock generating circuit enters an alarm state when the global synchronization signal is observed at time instants corresponding to more than one local clock cycle more or less than the number of local clock cycles.

28. (Previously Presented) The computer readable medium of claim 25 wherein the local clock generating circuit enters a missing clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle less than the number of local clock cycles.

29. (Previously Presented) The computer readable medium of claim 28 wherein the local clock generating circuit returns to the synchronization state from the missing clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle more than the number of local clock cycles.

30. (Previously Presented) The computer readable medium of claim 28 wherein the local clock generating circuit enters an alarm state from the missing clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one or more local clock cycle less than the number of local clock cycles.

31. (Previously Presented) The computer readable medium of claim 25 wherein the local clock generating circuit enters an extra clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle more than the number of local clock cycles.

32. (Previously Presented) The computer readable medium of claim 31 wherein the local clock generating circuit returns to the synchronization state from the extra clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle less than the number of local clock cycles.

33. (Previously Presented) The computer readable medium of claim 31 wherein the local clock generating circuit enters an alarm state from the extra clock state after an instance of the global synchronization signal is observed at a time instant corresponding to two or more local clock cycles more than the number of local clock cycles.

34. (Currently Amended) A system, comprising means for maintaining a synchronization state for a local clock generating means of a first of a number of components of a distributed system according to a number of local clock cycles recorded between successive occurrences of a global synchronization signal provided to each of the components of the distributed system,

wherein the synchronization state indicates that the local clock generating means is synchronized to the global synchronization signal,

wherein the local clock generating circuit can switch between a plurality of states, the plurality of states including the synchronization state, and an alarm state, and

wherein the components comprise line and/or switch cards of a communications switch.

35. (Previously Presented) The system of claim 34 wherein the local clock generating means enters the synchronization state only after observing a predetermined number of occurrences of successive local clock cycles between the successive occurrences of the global synchronization signal.

36. (Previously Presented) The system of claim 35 wherein the local clock generating means provides local control signals for the first of the components at time instants corresponding to the number of local clock cycles.

37. (Previously Presented) The system of claim 36 wherein the local clock generating means continues to provide local control signals for the first of the components at time instants corresponding to the number of local clock cycles even after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle more or less than the number of local clock cycles.

38. (Previously Presented) The system of claim 36 wherein the local clock generating means enters an alarm state when the global synchronization signal is observed at time instants corresponding to more than one local clock cycle more or less than the number of local clock cycles.

39. (Previously Presented) The system of claim 36 wherein the local clock generating means enters a missing clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle less than the number of local clock cycles.

40. (Previously Presented) The system of claim 39 wherein the local clock generating means returns to the synchronization state from the missing clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle more than the number of local clock cycles.

41. (Previously Presented) The system of claim 39 wherein the local clock generating means enters an alarm state from the missing clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one or more local clock cycle less than the number of local clock cycles.

42. (Previously Presented) The system of claim 36 wherein the local clock generating means enters an extra clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle more than the number of local clock cycles.

43. (Previously Presented) The system of claim 42 wherein the local clock generating means returns to the synchronization state from the extra clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle less than the number of local clock cycles.

44. (Previously Presented) The system of claim 42 wherein the local clock generating means enters an alarm state from the extra clock state after an instance of the global synchronization signal is observed at a time instant corresponding to two or more local clock cycles more than the number of local clock cycles.